

BUR9-1999-0300US1  
Amendment dated 01/07/2005

**AMENDMENT WITH RCE**

01240162aa  
Reply to office action mailed 09/07/2004

The following is a complete listing of all claims in the application, with an indication of the status of each:

**Listing of claims:**

1           1. (currently amended) A method of forming a field effect transistor (FET),  
2           comprising:  
3                 providing a substrate;  
4                 forming a layer on the substrate, the layer having exposed vertical side  
5           surfaces on opposite sides of the layer, the layer being able to support epitaxial  
6           growth on said side surfaces;  
7                 forming an epitaxial channel on each of the exposed vertical side  
8           surfaces of the layer, the channel having an exposed first vertical sidewall  
9           opposite the vertical side surface of the layer;  
10                removing a channel on a first vertical side surface of the layer and then  
11           removing the layer, thereby exposing a second vertical sidewall of the channel  
12           formed on the second vertical side of the layer;  
13                forming a second channel in place of said removed channel; and  
14                forming a gate adjacent to at least one of the sidewalls of the channel  
15           and the second channel, there being a gate dielectric between each channel and  
16           the gate.

1           2-13. (canceled)

1           14. (previously presented) A method for forming a double gated field effect  
2           transistor (FET), comprising the steps of:  
3                 forming on a substrate a first and a second epitaxially grown channels,  
4           said channels having vertical side surfaces extending up from the substrate,

5 wherein said second channel is grown following removal of a semiconductor  
6 region centered between said channels upon one of whose opposite vertical  
7 sides said first channel was grown;  
8 etching areas within a silicon layer to form a source and a drain,  
9 wherein a side surface of the source and the drain contact opposing end  
10 surfaces of the first and second epitaxially grown channels; and  
11 forming a gate that contacts a top surface and two side surfaces of the  
12 first and second epitaxially grown channels and a top surface of the substrate.

1 15. (previously presented) The method as recited in claim 14, wherein the  
2 forming step comprises the steps of:  
3 forming first and second semiconductor lines, each end of the silicon  
4 lines contacting an end of the source and the drain;  
5 forming an etch stop layer on an exposed side surface of each of the  
6 first and second semiconductor lines;  
7 epitaxially growing first and second semiconductor layers on each etch  
8 stop layer;  
9 etching away the first and second semiconductor lines and the etch  
10 stop layers;  
11 filling areas surrounding the first and second epitaxially grown  
12 semiconductor layers and between the source and the drain with an oxide fill;  
13 and  
14 etching a portion of the oxide fill to form an area that defines a gate,  
15 wherein the area that defines the gate is substantially centered between and  
16 substantially parallel to the source and the drain.

1 16. (original) The method as recited in claim 15, further comprising the steps  
2 of:

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3                   etching the oxide fill between the gate the source to expose the first  
4                   and second epitaxially grown silicon layers; and  
5                   etching the oxide fill between the gate and the drain to expose the first  
6                   and second epitaxially grown silicon layers.

1           17. (original) The method as recited in claim 16, further comprising the step  
2           of forming an oxide on the first and second epitaxially grown silicon layers.

1           18. (original) The method as recited in claim 17, wherein the oxide is silicon  
2           dioxide.

1           19. (previously presented) The method as recited in claim 14, further  
2           comprising the steps of:  
3                   implanting a portion of the epitaxially grown silicon layers between  
4                   the gate and the source; and  
5                   implanting a portion of the epitaxially grown silicon layers between  
6                   the gate and the drain.

1           20. (previously presented) The method as recited in claim 19, wherein the  
2           implanting step is in the range of 10 to 45 degrees relative to a vector  
3           perpendicular to a top surface of the epitaxially grown silicon layers.

1           21. (previously presented) The method as recited in claim 20, wherein the  
2           implants are done in a series at approximately 90 degrees relative to each  
3           other.

1           22. (original) The method as recited in claim 14, further comprising the step  
2           of forming a contact on each of the gate, the source and the drain.

1       23. (original) The method as recited in claim 14, wherein the gate material is  
2       polysilicon.

1       24. (currently amended) A method of forming an FET, comprising:  
2               forming on a substrate a first semiconductor layer having first and  
3       second ends and a central region that is thinner than said first and second ends,  
4       said central region having first and second side surfaces extending upward  
5       from said substrate, said semiconductor layer being able to support epitaxial  
6       growth on said first and second side surfaces;  
7               epitaxially growing a semiconductor channel region on at least one of  
8       said first and second side surfaces of said central region of said first  
9       semiconductor layer, a first side of said channel being exposed;  
10              removing said central region of said first semiconductor layer, thereby  
11       exposing a second side of said channel;  
12              forming a dielectric layer on exposed surfaces of said semiconductor  
13       channel region; and  
14              forming a gate electrode on said dielectric layer.

1       25. (previously presented) The method of claim 24, wherein said  
2       semiconductor channel region is formed of a combination of Group IV  
3       elements.

1       26. (previously presented) The method of claim 24, wherein said  
2       semiconductor channel region is formed of an alloy of silicon and a Group IV  
3       element.

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1        27. (previously presented) The method of claim 24, wherein said  
2        semiconductor channel region is formed of a material selected from the group  
3        consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

1        28. (previously presented) The method of claim 27, wherein said step of  
2        removing said first semiconductor layer does not appreciably remove said  
3        semiconductor channel region.

1        29. (previously presented) The method of claim 28, wherein an etch stop is  
2        epitaxially grown between said first semiconductor layer and said  
3        semiconductor channel region.

1        30 (previously presented) The method of claim 24, wherein said gate  
2        electrode is formed of a material selected from the group consisting of  
3        polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium  
4        nitride.